REMARKS/ARGUMENTS

In the Office Action mailed September 5, 2008, claims 1-7 were rejected. In response, Applicants hereby request reconsideration of the application in view of the proposed amendment and the below-provided remarks. No claims are added or cancelled. For reference, claim 1 includes a proposed amendment to correct a grammatical error.

Claim Rejections under 35 U.S.C. 103

Claims 1-7 were rejected under 35 U.S.C. 103(a) as being unpatentable over Murade (U.S. Pat. No. 6,531,996, hereinafter Murade) in view of Shimada et al. (U.S. Pat. No. 5,506,598, hereinafter Shimada). However, Applicants respectfully submit that these claims are patentable over Murade and Shimada for the reasons provided below.

Independent Claim 1

Claim 1 recites "an additional gate off supply line VLclean to substantially reduce a discharge time associated with driving transistors of the LC-Display, wherein the additional gate off supply line is coupled to the output stages of the gate drivers and is routed as a separate track from the gate off supply line VL" (emphasis added).

In contrast, neither Murade nor Shimada teaches an additional gate off supply line coupled to the output stages of a gate driver. The Office Action states that Murade does not explicitly teach an additional gate off supply line coupled to the output stages of the gate drivers. Office Action, page 3, paragraph 2. Shimada merely teaches using two bus lines connected to the gate electrodes of the transistors. Shimada, column 3, lines 5-9 ("A part of the gate bus line 101a functions as a gate electrode of TFT 103a and a part of gate bus line 101b functions as a gate electrode of TFT 103b." emphasis added). The lines connected to the gate electrodes of Shimada are different from lines connected to output stages because the function of gate electrodes is entirely different than the function of output stages. In general, a voltage applied to the gate electrode controls a current flowing through the output stages.

Shimada is merely concerned with using discrete bus lines connected to gates of TFTs to provide different voltages to different gates. Shimada, column 5, lines 61-64. Although Shimada mentions two gate bus lines, Shimada does not teach an additional gate off supply line coupled to the output stages of gate drivers.

For the reasons presented above, the combination of Shimada and Murade does not teach all of the limitations of the claim because neither Murade nor Shimada teaches an additional gate off supply line coupled to the output stages of a gate driver, as recited in the claim. Accordingly, Applicants respectfully assert claim 1 is patentable over Murade in view of Shimada because Murade and Shimada do not teach all of the limitations of the claim.

Independent Claim 6

Applicants respectfully assert independent claim 6 is patentable over the combination of Murade and Shimada at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 6 recites "providing an additional gate off supply line VLclean to substantially reduce a discharge time associated with driving transistors of the LC-Display, wherein the additional gate off supply line is coupled to the output stages of the gate drivers and is routed as a separate track from the gate off supply line VL" (emphasis added).

Here, although the language of claim 6 differs from the language of claim 1, and the scope of claim 6 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 6. Accordingly, Applicants respectfully assert claim 6 is patentable over the combination of Murade and Shimada because the combination of Murade and Shimada does not teach an additional gate off supply line coupled to the output stages of a gate driver.

Independent Claim 7

Applicants respectfully assert independent claim 7 is patentable over the combination of Murade and Shimada at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 7 recites "the

additional gate off supply line is coupled to the output stages of the gate drivers and is routed as a separate track from the gate off supply line VL" (emphasis added).

Here, although the language of claim 7 differs from the language of claim 1, and the scope of claim 7 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 7. Accordingly, Applicants respectfully assert claim 7 is patentable over the combination of Murade and Shimada because the combination of Murade and Shimada does not teach an additional gate off supply line coupled to the output stages of a gate driver.

Dependent Claims

Claims 2-5 depend from and incorporate all of the limitations of independent claim 1. Applicants respectfully assert claims 2-5 are allowable based on an allowable base claim. Additionally, each of claims 2-5 may be allowable for further reasons, as described below.

In regard to claim 4, Applicants respectfully submit that claim 4 is patentable over the combination of Murade and Shimada because the combination of cited references does not teach all of the limitations of the claim. Claim 4 recites "a track of the gate off supply line VL and a track of the additional supply line VLclean are coupled to a same supply level" (emphasis added). In contrast, the cited portion of Shimada (FIG. 7) is a graph that shows different voltages for different lines attached to gates. As discussed above in relation to claim 1, lines attached to gates are different from lines attached to output stages. Even if this citation were understood to teach additional lines connected to output stages, Shimada nevertheless explicitly states that the voltages applied to the lines must be different. Shimada, column 5, lines 9-15 ("As seen from FIG. 7, the electric potential of the gate bus line G(1,1) is set lower than that of the gate bus line G(1,2) by X V during the OFF period of the first field."). In fact, Shimada states that if the voltages over the different lines are the same, Shimada ceases to provide any benefit over the prior art devices. Shimada, column 3, lines 53-56. Thus, Shimada does not teach a gate off supply line and an additional gate off supply line coupled to a same supply level. Additionally, the Office Action does not assert that Murade might teach the missing

limitation of Shimada. Accordingly, Applicants respectfully assert that claim 4 is patentable over the combination of Murade and Shimada because Shimada does not teach a gate off supply line and an additional gate off supply line coupled to a same supply level, as recited in claim 4.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the proposed amendment and the remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,

/mark a. wilson/

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Mark A. Wilson
Reg. No. 43,994

Wilson & Ham
PMB: 348
2530 Berryessa Road
San Jose, CA 95132
Phone: (925) 249-1300
Fax: (925) 249-0111